REMARKS

The Office Action dated September 15, 2005, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Claim 9 has been amended. Claims 9-12 are pending in the present application.

Allowed Claims

Applicant appreciates the allowance of claims 10-13.

Claim 9 Rejected Under 35 U.S.C. § 102(b)

Claim 9 was rejected under 35 U.S.C. § 102(b) as being anticipated by Kojima et al. (U.S. Patent No. 5,995,429, hereinafter "Kojima"). Claim 9 has been amended. To the extent it is still relevant, Applicant respectfully traverses this rejection.

Claim 9 recites a method for conducting a multiple word line selection test comprising, among other features, a first step for generating a first reset signal using the first block control unit; a second step for inactivating multiple word lines in the first memory cell block and the sense amp group associated with the first memory cell block in response to the first reset signal; and a second step for generating a second reset signal using the second block control unit; a third step for inactivating multiple word lines in the second memory cell block and the sense amp group associated with the second memory cell block after performing the first step in response to the second reset signal.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicant's invention.

Kojima teaches a semiconductor memory device capable of conducting test operations includes a plurality of word drivers which keep word lines in an active state

when the word drivers are selected until the word drivers are reset. The semiconductor memory device of Kojima further includes a control circuit which successively selects more than one of the plurality of word drivers so as to achieve simultaneous activation of word lines corresponding to selected ones of the plurality of word drivers during the test operations.

Specifically, Kojima provides that,

> [[I]in order to perform a bank-interleave operation, the first bank 208 is selected, and a command ACT is input, so that 32 indicated word lines are successively and selectively activated, resulting in multiple activation of these word lines. Then, the second bank 208 is selected, and a command ACT is input, thereby achieving multiple activation of another 32 word lines. The same operations are performed up to the fourth bank 208.
>
> When multiple word lines are activated in all of the four banks 208, the first bank 208 is selected again, and a command PRE is input to deactivate the selected word lines. After this, the second bank 208 is chosen, and a command PRE is input, so that the selected word lines are deactivated. The same operations are performed with respect to the third and fourth banks 208. *See*, column 16, lines 14-29.

In essence, Kojima merely performs multiple activation of selected 32 word lines WL of a second bank 108, and then performs multiple activation of selected 32 word lines WL of a first bank 108 (activation is performed to a fourth bank in the embodiment), and deactivating the selected word lines WL from the first bank 108 to fourth bank 108 in units of bank.

However, the present invention generates a reset signal (WLrs, SArst) using a block control circuit (21) provided for each memory cell block (BL) and inactivates the multiple word lines in each memory cell block and a sense amp group in response to

the reset signal. As such, Applicant respectfully submits that Kojima fails to disclose or suggest each and every element recited in claim 9. For instance, Applicant submits that Kojima fails to disclose or suggest at least the features of "a first step for generating a first reset signal using the first block control unit; a second step for inactivating multiple word lines in the first memory cell block and the sense amp group associated with the first memory cell block in response to the first reset signal; and a second step for generating a second reset signal using the second block control unit; a third step for inactivating multiple word lines in the second memory cell block and the sense amp group associated with the second memory cell block after performing the first step in response to the second reset signal."

It is submitted that in order to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Kojima fails to disclose or suggest each and every feature of claim 9. Accordingly, Applicant respectfully submits that claim 9 is not anticipated by Kojima. Therefore, Applicant respectfully submits that claim 9 is allowable.

Accordingly, Applicant respectfully requests withdrawal of the rejection.

Conclusion

In view of the above, the Applicant respectfully requests allowance of claim 9 along with allowed claims 10-13 and the prompt issuance of a Notice of Allowability.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referencing Attorney Docket No. 108075-00124.

Respectfully submitted,

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Enclosure: Petition for Extension of Time (one month)